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EXAMINER

CHU, CHRIS C

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 07/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/082,500

Applicant(s)

CHIANG, CHENG-LIEN

Examiner

Chris C. Chu

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 01 May 2003 and 06 May 2003.
- 2a) ☒ This action is **FINAL**.      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 - 150 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 - 150 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 February 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 01 May 2003 is: a) ☒ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All   b) ☐ Some \*   c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)      4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)      5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_      6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Amendment***

1. Applicant's amendment filed on May 1, 2003 and May 6, 2003 have been received and entered in the case.

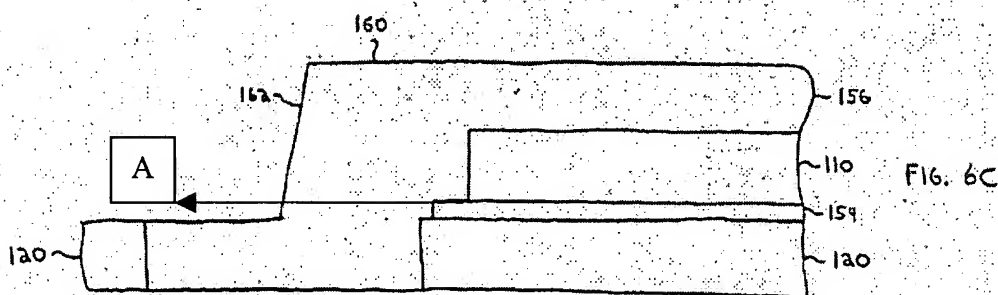
### ***Drawings***

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation in claims 3, 11 and 22 "the first housing portion is spaced from the upper surface," the limitation in claim 11, "a conductive trace that extends through an opening in the first housing portion," and the limitation in claims 16, 26, 36 and 46 "the insulative housing consisting of the first and second housing portions" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

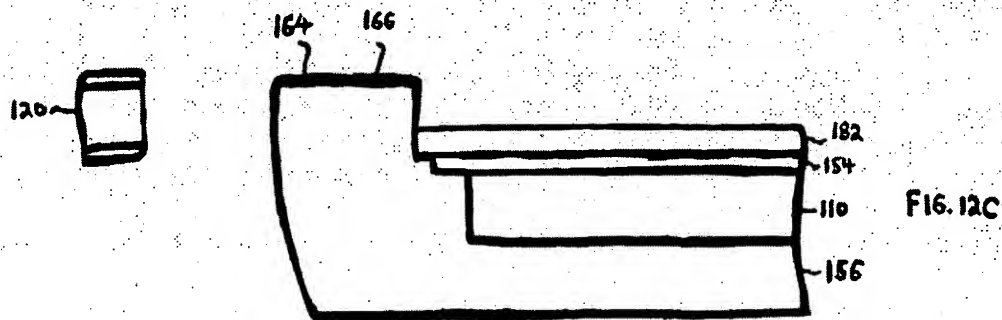
3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "132" in Fig. 2A and Fig. 2 has been used to designate both recessed portion and non-recessed portion, reference characters "156" and "166" in Fig. 6B have both been used to designate leads, reference characters "164" and "166" in Fig. 12C have both been used to designate top surfaces, and reference characters "184" and "186" in Fig. 13A have both been used to designate device. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.



On page 39, applicant argues "encapsulant 156 is spaced from surface 112 of chip 110, as shown in Figs. 6C, 6D, ... and 14B." This argument is not persuasive. As shown in the above

Fig. 6C, the area “A” clearly shows that the encapsulant 156 contacts the surface 112 of chip 110, not spaced from the surface 112 of the chip 110. Thus, the limitation in claims 3, 11 and 22 “the first housing portion is spaced from the upper surface,” is not shown in the figures.



Further, Fig. 12C clearly shows that the insulative housing does not consist of the first (156) and second (182) housing portions. Instead, Fig. 12C clearly shows the insulative housing containing the first (156), second (182) and third (154) housing portions. Thus, limitation in claims 16, 26, 36 and 46 “the insulative housing consisting of the first and second housing portions” is not shown in the figures.

Finally, applicant argues “the second housing portion is also illustrated by the combination of transparent adhesive 154 in Fig. 4A and transparent base 182 in Fig. 12B.” This argument is not persuasive because as disclosed by applicant on page 25, lines 20 ~ 25 of specification which clearly describes that the encapsulant (156) provides a first single-piece housing portion, the transparent base (182) provides a second single-piece housing portion, and the transparent adhesive (154) provides a third single-piece housing portion. Since applicant’s own specification clearly states that the second housing portion is the transparent base (182) and not a combination of transparent adhesive 154 in Fig. 4A and transparent base 182 in Fig. 12B,

limitation in claims 16, 26, 36 and 46 “the insulative housing consisting of the first and second housing portions” is not shown in the figures.

For the above reasons, the objections to the drawings are maintained.

### *Specification*

5. The disclosure is objected to because of the following informalities:

On page 7, the specification needs a brief description of the drawings for Figs. 1A ~ 14B.

Appropriate correction is required.

On page 42, applicant argues “the Brief Description of the Drawings need not describe each figure individually. For instance, no such requirement exists in the Rules or the Manual of Patent Examining Procedure. See 37 C.F.R. § 1.74 and M.P.E.P § 608.01(f).” This argument is not persuasive because the 37 C.F.R. § 1.74 and M.P.E.P § 608.01(f) clearly states that figures shall be correctly, concisely and accurately described in the brief description of the drawing (see M.P.E.P § 608.01(f) and 37 C.F.R. § 1.74). However, the sentence “FIGS. 1A – 14A are bottom perspective views that show a method of making an optoelectronic semiconductor package device in accordance with an embodiment of the present invention” is not clear or accurate description for the brief description of the drawings. Thus, Examiner recommends changing the brief description of the drawings. For example, Fig. 1A is a bottom perspective view of semiconductor chip, ... Fig. 14A is a bottom perspective view of an optoelectronic semiconductor package with bent leads, etc.

For the above reason, the objection to the specification is maintained.

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 76 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 76, line 3 from the bottom, the term “the planar metal trace contacts” lacks antecedent basis.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1 ~ 40, 61 ~ 63, 65, 71 ~ 73, 75 ~ 78, 80, 91 ~ 93, 95 ~ 98, 100, 111 ~ 113, 115 ~ 118, 120, 141 ~ 143, 145 ~ 148 and 150 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. in view of Fjelstad.

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Regarding claim 1, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface and a lower surface, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a first single-piece non-transparent insulative housing portion (27) that contacts the lower surface and is spaced from the light sensitive cell and a second transparent insulative housing portion (28) that contacts the first housing portion and the light sensitive cell, wherein the first housing portion includes a peripheral ledge, and the second housing portion is located within the peripheral ledge; and
- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the second housing portion being exposed. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has a second housing portion (235) being exposed. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).



Regarding claim 2, Nakamura et al. discloses in Fig. 2 the first housing portion contacting four outer side surfaces of the chip.

Regarding claim 3, Nakamura et al. discloses in Fig. 2 the first housing portion being spaced from the upper surface.

Regarding claim 4, Nakamura et al. discloses in Fig. 2 the second housing portion contacting the conductive trace.

Regarding claim 5, Nakamura et al. discloses in Fig. 2 the second housing portion being spaced from the lower surface.

Regarding claim 6, Nakamura et al. discloses in Fig. 2 the second housing portion being recessed relative to the peripheral ledge.

Regarding claims 7, 25 and 35, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric material. Further, the limitation “wherein the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric material” is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A “product by process” claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523;

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In re Fessmann, **180 USPQ 324**; In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a “product by, all of” claim, and not the patentability of the process, and that an old or obvious product, whether claimed in “product by process” claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 8, Nakamura et al. discloses in Fig. 2 the conductive trace extending through a peripheral side surface of the first housing portion and contacts the second housing portion without extending through a surface of the second housing portion.

Regarding claim 9, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

Regarding claim 10, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 11, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a first single-piece non-transparent insulative housing portion (27) that contacts the lower surface and the side surfaces and is spaced from the upper surface and a second transparent insulative housing

- portion (28) that contacts the first housing portion and the light sensitive cell and is spaced from the lower surface; and
- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a conductive trace that extends through an opening in the first housing portion. However, Fjelstad teaches in FIG. 5H a conductive trace (213) that extends through an opening (at the place of 235) in a first housing portion (240). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the conductive trace to be extending through an opening in the first housing portion as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct contact (column 2, lines 59 ~ 60).

Regarding claim 12, Nakamura et al., as modified, discloses in Fig. 2 the second housing portion including first and second opposing surfaces, the first surface contacts the light sensitive cell and being spaced from the conductive trace, and the second surface faces away from the chip. Nakamura et al., as modified, does not disclose a design of the insulative housing that is the second housing portion being exposed. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has a second housing portion (235) being exposed. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed as taught by Fjelstad. The ordinary artisan would have been motivated to further modify Nakamura et al. in the manner described

above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Regarding claim 13, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge, and the second housing portion being located within the peripheral ledge.

Regarding claim 14, Nakamura et al. discloses in Fig. 2 the second housing portion being recessed relative to the peripheral ledge.

Regarding claim 15, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric material. Further, the limitation “wherein the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric material” is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A “product by process” claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 116; In re Wertheim, 191 USPQ 90 (209 USPQ 254 does not deal with this issue); and In re Marosi et al., 218 USPQ 289 final product per se which must be determined in a “product by, all of” claim, and not the patentability

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of the process, and that an old or obvious product, whether claimed in “product by process” claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 16, Nakamura et al., as modified, discloses the insulative housing consisting of the first and second housing portions.

Regarding claim 17, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 the first housing portion being a transfer molded material that includes a peripheral ledge, and the second housing portion being a cured polymeric material that is located within the peripheral ledge and includes a first surface that contacts the light sensitive cell and is spaced from the conductive trace and a second surface opposite the first surface that faces away from the chip. Nakamura et al., as modified, does not disclose a design of the insulative housing that is the second housing portion being exposed. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has a second housing portion (235) being exposed. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed as taught by Fjelstad. The ordinary artisan would have been motivated to further modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41). Further, the limitation “wherein the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric material” is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability

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is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A “product by process” claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**; In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**; In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a “product by, all of” claim, and not the patentability of the process, and that an old or obvious product, whether claimed in “product by process” claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 18, Nakamura et al. discloses in Fig. 2 the conductive trace extending through a peripheral side surface of the first housing portion and contacting the second housing portion without extending through a surface of the second housing portion.

Regarding claim 19, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

Regarding claim 20, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 21, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

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- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a top surface, a bottom surface, wherein the insulative housing further includes first (27) and second (28) insulative housing portions, the first housing portion is a single-piece that provides the bottom surface and is non-transparent, and the second housing portion contacts the upper surface, is further from the bottom surface than the lower surface is from the bottom surface, provides at least a portion of the top surface and is transparent; and
- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the first insulative housing portion that has uncurved peripheral side surfaces between the top and bottom surfaces. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of the first insulative housing portion (240) that has uncurved peripheral side surfaces between top and bottom surfaces. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the first insulative housing portion to have uncurved peripheral side surfaces between the top and bottom surfaces as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of reducing a size of the semiconductor package.

Regarding claim 22, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces and being spaced from the upper surface.

Regarding claim 23, Nakamura et al. discloses in Fig. 2 the second housing portion contacting the light sensitive cell and the conductive trace and being spaced from the lower surface.

Regarding claim 24, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge that forms a peripheral portion of the top surface, and the second housing portion being located within and recessed relative to the peripheral ledge.

Regarding claim 26, Nakamura et al. discloses the claimed invention except for the insulative housing consisting of the first and second housing portions. However, Fjelstad teaches in FIG. 5H an insulative housing (240 and 235) consisting of the first (240) and second (235) housing portions. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the insulative housing consisting of the first and second housing portions as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Regarding claim 27, Nakamura et al. discloses in Fig. 2 the light sensitive cell contacting a major surface of the second housing portion that faces towards and being parallel to the upper surface.

Regarding claim 28, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through the top or bottom surfaces.

Regarding claim 29, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.



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Regarding claim 30, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 31, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first (27) and second (28) insulative housing portions, the first housing portion is a single-piece that provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface, contacts the lower surface and the outer side surfaces, is spaced from the light sensitive cell and is non-transparent, and the second housing portion is a single-piece or double-piece that provides a central portion of the top surface within the peripheral portion of the top surface, contacts the first housing portion, the light sensitive cell and the conductive trace, is spaced from the lower surface, is farther from the bottom surface than the lower surface is from the bottom surface, is transparent; and
- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the second housing portion being exposed. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an

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insulative housing (240 and 235) that has a second housing portion (235) being exposed. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Regarding claim 32, Nakamura et al., as modified, discloses the second housing portion including first and second opposing surfaces, the first surface faces towards the chip and contacts the light sensitive cell and is spaced from the conductive trace, and the second surface faces away from the chip and provides the central portion of the top surface and is exposed.

Regarding claim 33, Nakamura et al. discloses in Fig. 2 the peripheral portion of the top surface forming a rectangular peripheral ledge, and the second housing portion being located within and recessed relative to the peripheral ledge.

Regarding claim 34, Nakamura et al. discloses in Fig. 2 the peripheral ledge including four inner side surfaces that are opposite the peripheral side surfaces and outside a periphery of the chip.

Regarding claim 36, Nakamura et al., as modified, discloses the insulative housing consisting of the first and second housing portions.

Regarding claim 37, Nakamura et al., as modified, discloses in column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 the first housing portion being a transfer molded material that includes a peripheral ledge, and the second housing portion being a cured polymeric material that

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is located within the peripheral ledge and includes a first surface that faces towards the chip and contacts the light sensitive cell and is spaced from the conductive trace and a second surface opposite the first surface that faces away from the chip and provides the central portion of the top surface and is exposed. Further, the limitation “wherein the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric material” is a product-by-process claim language. Even though product- by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A “product by process” claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**; In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**; In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a “product by, all of” claim, and not the patentability of the process, and that an old or obvious product, whether claimed in “product by process” claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 38, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through the top or bottom surfaces.

Regarding claim 39, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through a surface of the second housing portion.

Regarding claim 40, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 61, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface and a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a first single-piece non-transparent insulative housing portion (27) that contacts the chip, covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion (28) that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface; and
- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the second housing portion being exposed and the conductive trace extending through an opening in the first housing portion. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has a second housing portion (235) being exposed and a conductive trace (213) extending through an opening (at the place of the 235) in a first housing portion (240). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed and the conductive trace extending through an

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opening in the first housing portion as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Regarding claim 62, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the side surfaces.

Regarding claim 63, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge, and the second housing portion being located within and recessed relative to the peripheral ledge.

Regarding claim 65, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 71, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface and a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a first single-piece non-transparent insulative housing portion (27) that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion (28) that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface; and

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- a conductive trace (22) that extends outside the insulative housing, and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the second housing portion being exposed; and the conductive trace extending through an opening in the first housing portion and does not contact an insulative material outside the first housing portion. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H and Fig. 7G-2 a design of an insulative housing (240 and 235) that has a second housing portion (235) being exposed; and a conductive trace (213) extending through an opening (at the place of 235) in a first housing portion (240) and does not contact an insulative material outside a first housing portion (240). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed; and the conductive trace extending through an opening in the first housing portion and does not contact an insulative material outside the first housing portion as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Regarding claim 72, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the side surfaces.

Regarding claim 73, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge, and the second housing portion being located within and recessed relative to the peripheral ledge.

Regarding claim 75, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 76, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a first single-piece non-transparent insulative housing portion (27) that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion (28) that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface; and
- a conductive trace (22 and 23) that includes a lead (22) and a planar metal traces (23), wherein the lead extends outside the insulative housing, and is electrically connected to the pad inside the insulative housing, and the planar metal trace contacts and is not integral with the lead, extends across one of the side surfaces and does not extend outside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the second housing portion being exposed and the lead extends through an opening in the first housing portion. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has a second housing portion (235) being exposed and a lead (213) extending through an opening (at the place of the 235) in a first housing portion (240). Thus, it would have

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been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed and the conductive trace extending through an opening in the first housing portion as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Regarding claim 77, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the side surfaces.

Regarding claim 78, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge, and the second housing portion being located within and recessed relative to the peripheral ledge.

Regarding claim 80, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 91, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first (27) and second (28) insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface



and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent; and

- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the top surface of the second housing portion being exposed. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has top surface of a second housing portion (235) being exposed. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Regarding claim 92, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces.

Regarding claim 93, Nakamura et al., as modified, discloses the conductive trace extending through an opening in one of the peripheral side surfaces.

Regarding claim 95, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

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Regarding claim 96, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first (27) and second (28) insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the first housing portion is exposed at the bottom surface and peripheral side surfaces; and
- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the first and second housing portion being exposed at the top surface. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has a first (240) and second (235) housing portion being exposed at the top surface. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by

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using the design of the insulative housing that has the first and second housing portion being exposed at the top surface as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Regarding claim 97, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces.

Regarding claim 98, Nakamura et al., as modified, discloses the conductive trace extending through an opening in one of the peripheral side surfaces.

Regarding claim 100, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 111, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first (27) and second (28) insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second

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- housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, and bottom surface and peripheral side surfaces are exposed; and
- a conductive trace (22) that extends outside the insulative housing, is located between the second housing portion and the chip inside the insulative housing, is spaced from the top surface and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the top surface being exposed. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has a top surface being exposed at the top surface. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the top surface being exposed as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Regarding claim 112, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces.

Regarding claim 113, Nakamura et al., as modified, discloses the conductive trace extending through an opening in one of the peripheral side surfaces.

Regarding claim 115, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 116, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

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- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first (27) and second (28) insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, and bottom surface and peripheral side surfaces are exposed; and
- a conductive trace (22) that extends outside the insulative housing, includes a top surface that faces away from the chip and contacts the second housing portion inside the insulative housing, includes a bottom surface that faces towards the chip and contacts the second housing portion inside the insulative housing, is spaced from the top and bottom surfaces, extends through one of the peripheral side surfaces and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the top surface being exposed. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has a top surface being exposed at the top surface. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify

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Nakamura et al. by using the design of the insulative housing that has the top surface being exposed as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Regarding claim 117, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces.

Regarding claim 118, Nakamura et al., as modified, discloses the conductive trace extending through an opening in one of the peripheral side surfaces.

Regarding claim 120, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 141, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes first (27) and second (28) insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing

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portion extends into the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip is transparent; and

- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the first insulative housing portion that has uncurved peripheral side surfaces between the top and bottom surfaces. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of the first insulative housing portion (240) that has uncurved peripheral side surfaces between top and bottom surfaces. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the first insulative housing portion to have uncurved peripheral side surfaces between the top and bottom surfaces as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of reducing a size of the semiconductor package.

Regarding claim 142, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces.

Regarding claim 143, Nakamura et al., as modified, discloses the conductive trace extending through an opening in one of the peripheral side surfaces.

Regarding claim 145, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 146, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

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- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes first (27) and second (28) insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, and the second housing portion extends into the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip is transparent, the first housing portion is exposed at the bottom surface and peripheral side surfaces; and
- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the first insulative housing portion that has uncurved peripheral side surfaces between the top and bottom surfaces and the first and second housing portion being exposed at the top surface. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of the first insulative housing portion (240) that has uncurved peripheral side surfaces between top and bottom surfaces and first (240) and second (235) housing portion being exposed at the top surface. Thus, it would have been obvious to one of ordinary skill in the art at



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the time when the invention was made to modify Nakamura et al. by using the design of the first insulative housing portion to have uncurved peripheral side surfaces between the top and bottom surfaces and the first and second housing portion being exposed at the top surface as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of reducing a size of the semiconductor package.

Regarding claim 147, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces.

Regarding claim 148, Nakamura et al., as modified, discloses the conductive trace extending through an opening in one of the peripheral side surfaces.

Regarding claim 150, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

10. Claims 41 ~ 51, 53 ~ 55 and 58 ~ 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. in view of Glenn et al.

Regarding claim 41, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface and a lower surface, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a top surface, a bottom surface and a peripheral side surface between the top and bottom surfaces,
- wherein the insulative housing further includes a first insulative housing portion (27) that covers the lower surface and is non-transparent and a second insulative housing portion (28) that covers the light sensitive cell and is transparent; and

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- a conductive trace (22) that protrudes laterally from and extends through the side surface and is electrically connected to the pad.

Nakamura et al. does not disclose the conductive trace including a recessed portion that extends into the insulative housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and the top surface. However, Glenn et al. discloses in Fig. 5 a conductive trace (30) including a recessed portion (33) that extends into an insulative housing (51) and is spaced from a top and bottom surfaces and a non-recessed portion (32) that extends outside the insulative housing and is adjacent to the recessed portion and the top surface. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the conductive trace as taught by Glenn et al. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of preventing the lead from being pulled vertically from the package (column 2, lines 22 and 23).

Regarding claim 42, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and four outer side surfaces of the chip.

Regarding claim 43, Nakamura et al. discloses in Fig. 2 the second housing portion contacting the light sensitive cell and the conductive trace.

Regarding claim 44, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge, and the second housing portion being located within the peripheral ledge.

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Regarding claims 45 and 55, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric material. Further, the limitation “wherein the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric material” is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A “product by process” claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**; In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**; In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a “product by, all of” claim, and not the patentability of the process, and that an old or obvious product, whether claimed in “product by process” claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 46, Nakamura et al. discloses in Fig. 2 the insulative housing consisting of the first and second housing portions.

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Regarding claim 47, Nakamura et al. discloses in Fig. 2 the light sensitive cell contacting a major surface of the second housing portion that faces towards and is parallel to the upper surface.

Regarding claim 48, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through the top or bottom surfaces.

Regarding claim 49, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through a surface of the second housing portion.

Regarding claim 50, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 51, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface and a lower surface, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a top surface, a bottom surface and a peripheral side surface between the top and bottom surfaces,
- wherein the insulative housing further includes a first single-piece housing portion (27) that contacts the lower surface and is spaced from the light sensitive cell and a second single-piece housing portion (28) that contacts the first housing portion and the conductive trace and is transparent, the first housing portion alone provides the bottom surface, and the first and second housing portions in combination provide the top surface; and

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- a conductive trace (22) that protrudes laterally from and extends through the side surface and is electrically connected to the pad.

Nakamura et al. does not disclose the conductive trace including a recessed portion that extends into the insulative housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and contacts the insulating housing, wherein the recessed and non-recessed portions each include four outer surfaces, three of the outer surfaces of the recessed and non-recessed portions that do not face in the same direction as the top surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and one of the outer surfaces of the recessed and non-recessed portions that face in the same direction as the top surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another. However, Glenn et al. discloses in Fig. 5 a conductive trace (30) including a recessed portion (33) that extends into an insulative housing (51) and is spaced from a top and bottom surfaces and a non-recessed portion (32) that extends outside the insulative housing and is adjacent to the recessed portion and contacts the insulating housing, wherein the recessed and non-recessed portions each include four outer surfaces, three of the outer surfaces of the recessed and non-recessed portions that do not face in the same direction as the top surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and one of the outer surfaces of the recessed and non-recessed portions that face in the same direction as the top surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the

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conductive trace as taught by Glenn et al. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of preventing the lead from being pulled vertically from the package (column 2, lines 22 and 23).

Regarding claim 53, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge, and the second housing portion being located within and recessed relative to the peripheral ledge.

Regarding claim 54, Nakamura et al. discloses in Fig. 2 the peripheral ledge including four inner side surfaces that are opposite the peripheral side surfaces and outside a periphery of the chip.

Regarding claim 58, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through the top or bottom surfaces.

Regarding claim 59, Nakamura et al. discloses in Fig. 2 the device being devoid of an electrical conductor that extends through opposing surfaces of the second housing portion.

Regarding claim 60, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

11. Claims 52, 56 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. and Glenn et al. as applied to claim 51 above, and further in view of Fjelstad.

Regarding claim 52, Nakamura et al., as modified, discloses in Fig. 2 the second housing portion including first and second opposing surfaces, the first surface contacts the light sensitive cell and being spaced from the conductive trace, and the second surface faces away from the chip. Nakamura et al., as modified, does not disclose a design of the insulative housing that is the

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second housing portion being exposed. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has a second housing portion (235) being exposed. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed as taught by Fjelstad. The ordinary artisan would have been motivated to further modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Regarding claim 56, Nakamura et al., as modified, discloses the claimed invention except for the insulative housing consisting of the first and second housing portions. However, Fjelstad teaches in FIG. 5H an insulative housing (240 and 235) consisting of the first (240) and second (235) housing portions. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the insulative housing consisting of the first and second housing portions as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Regarding claim 57, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 the first housing portion being a transfer molded material that includes a peripheral ledge, and the second housing portion being a cured polymeric material that is located within the peripheral ledge and includes a first surface that contacts the light sensitive cell and is spaced from the conductive trace and a second surface opposite the first surface that

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faces away from the chip. Nakamura et al., as modified, does not disclose a design of the insulative housing that is the second housing portion being exposed. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has a second housing portion (235) being exposed. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed as taught by Fjelstad. The ordinary artisan would have been motivated to further modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41). Further, the limitation “wherein the first housing portion being a transfer molded material, and the second housing portion being a cured polymeric material” is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A “product by process” claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**; In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**; In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a “product by, all of” claim, and not the patentability of the process, and that an old or obvious product, whether claimed in “product by process”



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claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

12. Claims 64, 66 ~ 70, 74, 79, 94, 99, 114, 119, 144 and 149 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. in view of Fjelstad as applied to claims 61, 71, 76, 91, 96, 111, 116, 141 and 146 above, and further in view of Glenn et al.

Regarding claims 64, 69, 74, 79, 94, 99, 114, 119, 144 and 149, Nakamura et al., as modified, discloses the claimed invention except for the conductive trace including a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion. However, Glenn et al. discloses in Fig. 5 a conductive trace (30) including a recessed portion (33) and a non-recessed portion (32), the recessed portion extends into an insulative housing (51), the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions

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are adjacent to one another, and an opening (at the place around 30) includes sidewalls that contact and span 360 degrees around the recessed portion. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Nakamura et al. by using the conductive trace as taught by Glenn et al. The ordinary artisan would have been motivated to further modify Nakamura et al. in the manner described above for at least the purpose of preventing the lead from being pulled vertically from the package (column 2, lines 22 and 23).

Regarding claim 66, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a first single-piece non-transparent insulative housing portion (27) that contacts the chip, covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion (28) that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface; and
- a conductive trace (22) that extends through an opening in the first housing portion, extends outside the insulative housing, and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the second housing portion being exposed. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an

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insulative housing (240 and 235) that has a second housing portion (235) being exposed. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Further, Nakamura et al., as modified, does not disclose the conductive trace being bent outside the insulative housing. However, Glenn et al. discloses in Fig. 5 a conductive trace (30) being bent outside the insulative housing (51). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Nakamura et al. by using the conductive trace as taught by Glenn et al. The ordinary artisan would have been motivated to further modify Nakamura et al. in the manner described above for at least the purpose of strengthening the solder connection (column 3, lines 11 ~ 15).

Regarding claim 67, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the side surfaces.

Regarding claim 68, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge, and the second housing portion being located within and recessed relative to the peripheral ledge.

Regarding claim 70, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

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13. Claims 81 ~ 83, 85 ~ 88 and 90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. in view of Fjelstad, and further in view of Tsuji et al.

Regarding claim 81, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a first single-piece non-transparent insulative housing portion (27) that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion (28) that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface; and
- a conductive trace (22 and 23) that includes a lead (22) and a planar metal traces (23), wherein the lead extends outside the insulative housing, and is electrically connected to the pad inside the insulative housing, and the planar metal trace contacts and is not integral with the lead, extends across one of the side surfaces and does not extend outside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the second housing portion being exposed and the lead extends through an opening in the first housing portion. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has a second housing portion (235) being exposed and a lead (213) extending through an opening (at the place of the 235) in a first housing portion (240). Thus, it would have

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been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed and the conductive trace extending through an opening in the first housing portion as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Further, Nakamura et al., as modified, does not disclose the planar metal trace contacting the first and second housing portions. However, Tsuji et al. discloses in Fig. 18A a planar metal trace (52) contacting first (23) and second (53) housing portions. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Nakamura et al. by using the planar metal trace as taught by Tsuji et al. The ordinary artisan would have been motivated to further modify Nakamura et al. in the manner described above for at least the purpose of coping with different sizes of semiconductor chips (column 2, lines 57 ~ 61).

Regarding claim 82, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the side surfaces.

Regarding claim 83, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge, and the second housing portion being located within and recessed relative to the peripheral ledge.

Regarding claim 85, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

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Regarding claim 86, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a first single-piece non-transparent insulative housing portion (27) that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion (28) that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface; and
- a conductive trace (22 and 23) that includes a lead (22) and a planar metal traces (23), wherein the lead extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, and the planar metal trace contacts and is not integral with the lead, overlaps the pad, extends across one of the side surfaces and does not extend outside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the second housing portion being exposed and the lead extends through an opening in the first housing portion. However, Fjelstad teaches in FIG. 5F ~ FIG. 5H a design of an insulative housing (240 and 235) that has a second housing portion (235) being exposed and a lead (213) extending through an opening (at the place of the 235) in a first housing portion (240). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the second housing

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portion being exposed and the conductive trace extending through an opening in the first housing portion as taught by Fjelstad. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of providing a direct thermal path to facilitate the removal of heat from the packaged chips (column 1, lines 39 ~ 41).

Further, Nakamura et al., as modified, does not disclose the planar metal trace contacting the first and second housing portions. However, Tsuji et al. discloses in Fig. 18A a planar metal trace (52) contacting first (23) and second (53) housing portions. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Nakamura et al. by using the planar metal trace as taught by Tsuji et al. The ordinary artisan would have been motivated to further modify Nakamura et al. in the manner described above for at least the purpose of coping with different sizes of semiconductor chips (column 2, lines 57 ~ 61).

Regarding claim 87, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the side surfaces.

Regarding claim 88, Nakamura et al. discloses in Fig. 2 the first housing portion including a peripheral ledge, and the second housing portion being located within and recessed relative to the peripheral ledge.

Regarding claim 90, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

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14. Claims 84 and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al., Fjelstad and Tsuji et al. as applied to claims 81 and 86 above, and further in view of Glenn et al.

Regarding claims 84 and 89, Nakamura et al., as modified, discloses the claimed invention except for the conductive trace including a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion. However, Glenn et al. discloses in Fig. 5 a conductive trace (30) including a recessed portion (33) and a non-recessed portion (32), the recessed portion extends into an insulative housing (51), the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and an opening (at the place around 30) includes sidewalls that contact and span 360 degrees around the recessed portion. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Nakamura et al. by using the



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conductive trace as taught by Glenn et al. The ordinary artisan would have been motivated to further modify Nakamura et al. in the manner described above for at least the purpose of preventing the lead from being pulled vertically from the package (column 2, lines 22 and 23).

15. Claims 101 ~ 103, 105 ~ 108, 110, 121 ~ 123, 125 ~ 128, 130 ~ 133, 135 ~ 138 and 140 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. in view of Tsuji et al.

Regarding claim 101, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first (27) and second (28) insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent; and

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- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the second housing portion being exposed at the top surface and the central portion of the top surface being recessed relative to the peripheral portion of the top surface. However, Tsuji et al. teaches in FIG. 26A an column 23, lines 33 ~ 34 a design of an insulative housing (92 and 95) that has a second housing portion (95) being exposed at the top surface and a central portion of the top surface being recessed relative to the peripheral portion of the top surface. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being exposed at the top surface as taught by Tsuji et al. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of increasing reliability of the semiconductor package (column 2, lines 29 ~ 30).

Regarding claim 102, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces.

Regarding claim 103, Nakamura et al., as modified, discloses the conductive trace extending through an opening in one of the peripheral side surfaces.

Regarding claim 105, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 106, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

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- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first (27) and second (28) insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the first housing portion is exposed at the bottom surface and peripheral side surfaces; and
- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the first and second housing portion being exposed at the top surface and the central portion of the top surface being recessed relative to the peripheral portion of the top surface. However, Tsuji et al. teaches in FIG. 26A an column 23, lines 33 ~ 34 a design of an insulative housing (92 and 95) that has a first (92) and second (95) housing portion being exposed at the top surface and a central portion of the top surface being recessed relative to the peripheral portion of the top surface. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was

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made to modify Nakamura et al. by using the design of the insulative housing that has the first and second housing portion being exposed at the top surface as taught by Tsuji et al. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of increasing reliability of the semiconductor package (column 2, lines 29 ~ 30).

Regarding claim 107, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces.

Regarding claim 108, Nakamura et al., as modified, discloses the conductive trace extending through an opening in one of the peripheral side surfaces.

Regarding claim 110, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 121, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes first (27) and second (28) insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are

spaced from the bottom surface and is non-transparent, and the second housing portion is located within the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip is transparent; and

- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that has the second housing portion being recessed relative to the peripheral ledge. However, Tsuji et al. teaches in FIG. 26A an column 23, lines 33 ~ 34 a design of an insulative housing (92 and 95) that has a second housing portion (95) being recessed relative to the peripheral ledge. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being recessed relative to the peripheral ledge as taught by Tsuji et al. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of increasing reliability of the semiconductor package (column 2, lines 29 ~ 30).

Regarding claim 122, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces.

Regarding claim 123, Nakamura et al., as modified, discloses the conductive trace extending through an opening in one of the peripheral side surfaces.

Regarding claim 125, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 126, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes first (27) and second (28) insulative housing portions, wherein the first housing portion is a single-piece that includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, the second housing portion is located within the peripheral ledge, contacts the light sensitive cell, does not extend midway between the upper and lower surfaces outside the chip is transparent, the first housing portion is exposed at the bottom surface and peripheral side surfaces; and
- a conductive trace (22) that extends outside the insulative housing, includes a top surface that faces away from the chip and contacts the second housing portion inside the insulative housing, includes a bottom surface that faces towards the chip and contacts the second housing portion inside the insulative housing, is spaced from the top and bottom surfaces, extends through one of the peripheral side surfaces and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the first and second housing portion being exposed at the top surface and the second housing portion being recessed relative to the peripheral ledge. However, Tsuji et al. teaches in FIG. 26A an column 23, lines 33 ~ 34 a design of an insulative housing (92 and 95) that has a first (92) and second (95) housing portion being exposed at the top surface and a second housing portion being recessed relative to the peripheral ledge. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the first and second housing portion being exposed at the top surface and the second housing portion being recessed relative to the peripheral ledge as taught by Tsuji et al. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of increasing reliability of the semiconductor package (column 2, lines 29 ~ 30).

Regarding claim 127, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces.

Regarding claim 128, Nakamura et al., as modified, discloses the conductive trace extending through an opening in one of the peripheral side surfaces.

Regarding claim 130, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 131, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

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- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes first (27) and second (28) insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, the second housing portion is located within the peripheral ledge, contacts the light sensitive cell and the inner side surface, does not extend midway between the upper and lower surfaces outside the chip is transparent; and
- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the second housing portion being recessed relative to the peripheral ledge. However, Tsuji et al. teaches in FIG. 26A an column 23, lines 33 ~ 34 a design of an insulative housing (92 and 95) that has a second housing portion (95) being recessed relative to the peripheral ledge. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the second housing portion being recessed relative to the peripheral ledge as taught by Tsuji et al. The ordinary



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artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of increasing reliability of the semiconductor package (column 2, lines 29 ~ 30).

Regarding claim 132, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces.

Regarding claim 133, Nakamura et al., as modified, discloses the conductive trace extending through an opening in one of the peripheral side surfaces.

Regarding claim 135, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 136, Nakamura et al. discloses in Fig. 2, column 9, lines 12 ~ 19 and column 12, lines 11 ~ 16 an optoelectronic semiconductor package device, comprising:

- a semiconductor chip (26) that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell (29) and a conductive pad (25);
- an insulative housing (27 and 28) that includes first (27) and second (28) insulative housing portions, wherein the first housing portion is a single-piece that covers the lower surface and the outer side surfaces and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards the bottom surface and are spaced from the bottom surface and is non-transparent, the second housing portion is located within the peripheral ledge, contacts the light sensitive cell and the inner side

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- surface, does not extend midway between the upper and lower surfaces outside the chip is transparent, the first housing portion is exposed at the bottom surface and peripheral side surfaces; and
- a conductive trace (22) that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Nakamura et al. does not disclose a design of the insulative housing that is the first and second housing portion being exposed at the top surface and the second housing portion being recessed relative to the peripheral ledge. However, Tsuji et al. teaches in FIG. 26A an column 23, lines 33 ~ 34 a design of an insulative housing (92 and 95) that has a first (92) and second (95) housing portion being exposed at the top surface and a second housing portion being recessed relative to the peripheral ledge. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakamura et al. by using the design of the insulative housing that has the first and second housing portion being exposed at the top surface and the second housing portion being recessed relative to the peripheral ledge as taught by Tsuji et al. The ordinary artisan would have been motivated to modify Nakamura et al. in the manner described above for at least the purpose of increasing reliability of the semiconductor package (column 2, lines 29 ~ 30).

Regarding claim 137, Nakamura et al. discloses in Fig. 2 the first housing portion contacting the lower surface and the outer side surfaces.

Regarding claim 138, Nakamura et al., as modified, discloses the conductive trace extending through an opening in one of the peripheral side surfaces.

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Regarding claim 140, Nakamura et al. discloses in Fig. 2 the device being devoid of wire bonds, TAB leads and solder joints.

16. Claims 104, 109, 124, 129, 134 and 139 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. and Tsuji et al. as applied to claims 101, 106, 121, 126, 131 and 136 above, and further in view of Glenn et al.

Regarding claims 104, 109, 124, 129, 134 and 139, Nakamura et al., as modified, discloses the claimed invention except for the conductive trace including a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

However, Glenn et al. discloses in Fig. 5 a conductive trace (30) including a recessed portion (33) and a non-recessed portion (32), the recessed portion extends into an insulative housing (51), the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one

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another, and an opening (at the place around 30) includes sidewalls that contact and span 360 degrees around the recessed portion. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Nakamura et al. by using the conductive trace as taught by Glenn et al. The ordinary artisan would have been motivated to further modify Nakamura et al. in the manner described above for at least the purpose of preventing the lead from being pulled vertically from the package (column 2, lines 22 and 23).

### *Response to Arguments*

17. Applicant's arguments with respect to claims 1, 6, 9, 11, 12, 13, 15, 17, 19, 21, 25, 27, 29, 31, 41, 45, 47, 49, 51, 52, 57 and 59 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

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will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

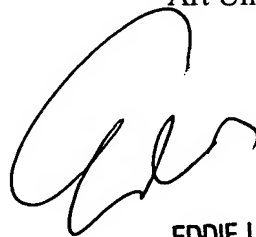
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu  
Examiner  
Art Unit 2815

c.c.  
July 25, 2003



EDDIE LEE  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800